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WEAVER AUSTIN VILLENEUVE & SAMPSON LLP - ALTERA
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER
YAARY, MICHAEL D

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)	
Office Action Summary	10/804,294	ESPOSITO ET AL.	
	Examiner	Art Unit	
	MICHAEL YAARY	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>04 December 2008</u>.
2a) ☐ This action is **FINAL.**   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
      closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-30</u> is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) <u>1-30</u> is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All b) ☐ Some * c) ☐ None of:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. _____.
    3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
         application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-30 are pending in the application.

2.   Applicant's request for reconsideration of the finality of the rejection of the last

Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

3.   Applicant argues that A) there is no suggestion or motivation to combine the

references of Magesacher and Barnette as applied to claim 1 and that the references

teach away from each other; B) AAPA does not teach "...at least M delay elements,

each delay element of the plurality delaying each of the M channel's data and providing

an output that is specific to an individual channel of the M channels," as in claim 5; and

C) Hyatt does not teach "a multiplexer that multiplexes M channels and provides a

multiplexed signal to the integrator," as in claim 6.

4.   As to argument A) examiner respectfully disagrees. Both references are

analogous in that the teach methods of interpolation using filters. Thus, both references

are able to be taken in combination with proper motivation to do so. Therefore,

Magesacher when taken in combination with the teachings of Barnette disclose the

limitations of claim 1. As in the rejection, Magesacher is silent to the limitation of a

plurality of delay elements connected in series between the delay section input and the

delay section output. Magesacher teaches the delay section, however, does not

disclose the plurality of delay elements. Barnette teaches of an interpolation filter

comprising multiple input signals and multiple delay stages in series providing

appropriate filtering and other interpolation functions. Thus, there is significant

motivation for one of ordinary skill in the art at the time of the invention to make the

combination. An example would to provide an increased flexibility in processing of

multiple inputs as different delays are applied to the different inputs as shown in figure 5

of Barnette. As a result this variable delay when taken in combination with Magesacher

would apply to the multiple signal paths as shown in Magesacher.

5.   As to argument B) examiner respectfully disagrees. Applicant is reminded that it

is the combination of Magesacher, Barnette and AAPA (applicant admitted prior art) that

teach the limitations of claim 5. Examiner points to the rejection of the claim in which

Barnette teaches the claimed plurality of delay elements, not AAPA as misinterpreted by

the applicant.

6.   As to argument C) examiner respectfully disagrees. Hyatt teaches the

multiplexing signals on a plurality of channels. Thus when taken the integrator taught in

the combination of Magesacher, Barnette, and AAPA, the combination teaches the

claimed limitations. Motivation to make the combination is found in the rejection of the

claim.

Claim Rejections - 35 USC § 103

7.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

8.   Claims 1, 7, 11, 15, 18, 22, 29, and 30 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Magesacher et al. (hereafter Magesacher)(US Pat. 6,829,629)

in view of Barnette (US Pat. 6,970,511).

9.   Magesacher and Barnette were cited in the previous office action dated

10/27/2008.

10.   **As to claim 1,** Magesacher discloses a multi-channel integrator (integrator of

figure 1) comprising:

        An integrator input (input xi of figure 1);

        An integrator output (output of integrator in figure 1);

        An adder (adder 12 of figure 1) comprising:

A first adder input connected to the integrator input (input xi connected to

adder 12 in figure 1);

A second adder input (second input of adder 12 in figure 1); and

An adder output (output of adder 12 in figure 1);

A delay section (delay stage 14 in figure 1) comprising:

A delay section input (input to delay stage 14 in figure 1);

A delay section output (output to delay stage 14 in figure 1);

A feedback line connecting the delay section output to the second adder input

(delay output feedback to adder 12 second input in figure 1);

Wherein the adder output is connected to the delay section input (adder output

connected to delay stage input in delay stage 12 in figure 1); and

Further wherein the delay section output is connected to the integrator output

(Integrator of figure 1 comprises multiple identical delay stages, the last delay stage 14

having an output connected to the integrator output.).

11.   Magesacher does not disclose that the delay section comprises a plurality of

delay elements connected in series between the delay section input and the delay

section output.

However, in an analogous art, Barnette discloses a plurality of delay elements

connected in series between the delay section input and the delay section output

(Figure 5 and column 15, lines 64-67 disclose a delay section with multiple delay

elements.).

12.   Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Magesacher, by implementing a plurality of delay elements as taught by Barnette, for the benefit of being able to specifically control sampling delay time, as each delay element delays the input signal by one sample delay (Barnette, column 15, lines 64-67). One would be motivated to make the combination as to control a decimation sequence of input signals and to provide more flexibility in delay time by allowing multiple inputs to be processed with different delays. The various delays would allow, as a result, for versatility in the different filtering functions of the different input channels.

13.   **As to claim 15,** Magesacher discloses a multi-channel differentiator (differentiator 16 in figure 2) comprising:

A differentiator input (input to differentiator circuit in figure 1);

A differentiator output (output yi to differentiator circuit in figure 1);

A subtractor (subtractor 128 in figure 2) comprising:

A first subtractor input (subtractor input to subtractor 128);

A second subtractor input (second subtractor input to subtractor 128);

A subtractor output (output of subtractor 128);

A delay section (delay section 130 in figure 1) comprising:

A delay section input connected to the differentiator input (differentiator input connected to delay element 130 input in figure 1);

A delay section output (output of delay element 130);

A feedforward line connecting the differentiator input to the first subtractor input (feedforward line to subtractor 128 in figure 1);

Wherein the delay section output is connected to the second subtractor input (delay section 130 output connected to subtractor 128 input in figure 1); and

Wherein the subtractor output is connected to the differentiator output (Differentiator of figure 1 comprises multiple identical delay stages, the last delay stage 14 having an output connected to the differentiator output).

9. Magesacher does not disclose that the delay section comprises a plurality of delay elements connected in series between the delay section input and the delay section output.

However, in an analogous art, Barnette discloses a plurality of delay elements connected in series between the delay section input and the delay section output (Figure 5 and column 15, lines 64-67 disclose a delay section with multiple delay elements.).

14.   Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Magesacher, by implementing a plurality of delay elements as taught by Barnette, for the benefit of being able to specifically control sampling delay time, as each delay element delays the input signal by one

sample delay (Barnette, column 15, lines 64-67). One would be motivated to make the combination as to control a decimation sequence of input signals.

15.   **As to claim 7 and 11,** the combination of Magesacher and Barnette disclose at least N instances of integrator of claim 1 in series (Multiple instances in the integrator and differentiator of figure 1).

16.   **As to claims 18 and 22,** the combination of Magesacher and Barnette disclose at least N instances of differentiator of claim 15 in series (Multiple instances in the integrator and differentiator of figure 1).

17.   **As to claim 29,** the claim is rejected for the same reasons as claim 1 above.

18.   **As to claim 30,** the claim is rejected for the same reasons as claim 15 above.

19.   Claims 13, 14, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magesacher and Barnette as applied to claims 1 and 15 above, and further in view of McCaslin et al. (hereafter McCaslin)(US Pat. 4,999,798).

20.   McCaslin was cited in the previous office action dated 02/20/2008

21.   **As to claim 13,** the combination of Magesacher and Barnette do not disclose the

integrator is implemented in a programmable device.

   However, McCaslin discloses integrator is implemented in a programmable

device (column 5, lines 52-57).

22.   Therefore, it would have been obvious to one of ordinary skill in the art to modify

the teachings of Magesacher, Barnette, by implementing the circuit in a programmable

device, as taught by McCaslin, in order to be able to reconfigure the device as

necessary.

23.   **As to claim 14,** the combination of Magesacher, Barnette, and McCaslin

disclose the delay section is implemented in one or more embedded memory blocks in

a programmable device (Inherent in the delay elements of McCaslin figure 2, as they

need to be embedded in memory in order to operate.).

24.   **As to claims 24 and 25,** the claims are rejected for the same reasons as claims

13 and 14 respectively.

25.   Claims 2-5, 8-10, 12, 16, 19, 20, 21 and 23 are rejected under 35 U.S.C. 103(a)

as being unpatentable over Magesacher in view of Barnette and further in view of

Applicant admitted prior art (hereafter AAPA).

26.   **As to claim 2,** the combination of Magesacher and Barnette do not disclose a

multi-channel numerically controlled oscillator comprising the integrator of claim 1.

       However, AAPA discloses a multi-channel numerically controlled oscillator

comprising the integrator of claim 1 (Page 5, lines 11-28, disclose a standard multi-

channel numerically controlled oscillator).

27.   Therefore, it would have been obvious to one of ordinary skill in the art at the

time of the invention to modify the teachings of Magesacher and Barnett, by

incorporating a numerically controlled oscillator with integrators and differentiators, as

taught by AAPA for the benefit of generating sinusoidal signals of desired frequencies

for various functions in programmable devices (AAPA page 5, lines 12-13). One would

be motivated to make the combination, as an NCO is a standard known device to one of

ordinary skill in the art to be used to generate a desired frequency.

28.   **As to claim 3,** the combination of Magesacher, Barnette, and AAPA disclose a

phase incrementer input multiplexer connected to the integrator input (AAPA, phase

incrementer inputs 302a-302N in figure 3B); and

       A sine/cosine generation unit connected to the integrator output (sine/cosine

generator in figure 3B).

29.   **As to claims 4, 5, 8, 9, and 12,** the combination of Magesacher, Barnette, and

AAPA disclose the numerically controlled oscillator is an M channel numerically

controlled oscillator (AAPA, inputs from 302a-302N thus having M channels) and the

delay section of the integrator comprises at least M delay elements in series, wherein

each element of the plurality of delay elements delaying each of the M channel's data

and providing an output that is specific to an individual channel of the M channels

(Barnette, figure 5 discloses different delay elements 506, 511, and 516 in the delay

section providing delays to each of the input signals and providing specific output.).

30.   **As to claim 10,** the combination of Magesacher, Barnette, and AAPA disclose

an up-sampler having an up-sampler output connected to the integrator input and an

up-sampler input; and a differentiator connected to the up-sampler input (AAPA,

interpolator of Figure 1B).

31.   **As to claims 16, 19, 20 and 23,** the claims are rejected for the same reasons as

claim 5, 8, 9, and 12 above as applied to the differentiator circuit of figure 1 of

Magesacher.

32.   **As to claim 21,** the claim is rejected for the same reasons as claim 10 above.

33.   Claims 6, 17, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magesacher in view of Barnette and AAPA, and further in view of Hyatt (US Pat. 4,686,655).

34.   Hyatt was cited in the previous office action dated 10/27/2008.

35.   **As to claim 6,** the combination of Magesacher, Barnette, and AAPA disclose a down sampler having a down-sampler input connected to the integrator output and a down-sampler output; and a differentiator connected to the down-sampler output (AAPA, decimator of Figure 1A).

36.   The combination of Magesacher, Barnette, and AAPA do not disclose a multiplexer that multiplexes M channels and provides a multiplexed signal to the integrator.

        However, Hyatt discloses a multiplexer that multiplexes M channels and provides a multiplexed signal to the integrator (Column 43, lines 27-53 and column 60, lines 7-11 disclose a filtering apparatus multiplexing M signal channels for operation. Thus, when the teachings of Hyatt are combined with the teachings of Magesacher, Barnette, and AAPA the signal multiplexing can be used with the integrator to provide a multiplexed signal processing environment.).

37.   Therefore, it would have been obvious to one of ordinary skill in the art at the

time of the invention, to modify the teachings of Magesacher, Barnette, and AAPA by

utilizing the multiplexer, as taught by Hyatt, for the benefit of creating more flexibility by

combining and selecting signals used in the filter as a multiplexer would allow for an

appropriate signal to be selected in the multi-signal filtering system.

38.   **As to claim 17,** the claim is rejected for the same reasons as claim 6 above.

39.   **As to claim 26,** the claim is rejected for the same reasons as claims 1, 6, and 15

above, but the combination of Magesacher, Barnette, and AAPA do not disclose the

integration section comprises a multiplexer comprising M multiplexer inputs and a

multiplexer output.

        However, Hyatt discloses the integrator section comprising a multiplexer

comprising M multiplexer inputs and a multiplexer output (Column 43, lines 27-53 and

column 60, lines 7-11 disclose a filtering apparatus multiplexing M signal channels for

operation. Thus, when the teachings of Hyatt are combined with the teachings of

Magesacher, Barnette, and AAPA the signal multiplexing can be used with the

integrator to provide a multiplexed signal processing environment.).

40.   Therefore, it would have been obvious to one of ordinary skill in the art at the

time of the invention to modify the teachings of Magesacher, Barnette, and AAPA, by

utilizing a multiplexer for the input signals, as taught by Hyatt, for the benefit of being

able to selectively communicate data accordingly and for creating more flexibility by

combining and selecting signals used in the filter as a multiplexer would allow for an

appropriate signal to be selected in the multi-signal filtering system.

41.   **As to claim 27,** the claim is rejected for the same reasons as claim 26 above

and for the same reasons as recited in claim 10 above as the combination of

Magesacher, Barnette, and AAPA would achieve the same predictable filtering result

when combined with the teachings of Hyatt.

42.   **As to claims 28,** the claim is rejected for the same reasons as claims 1-3 and 26

above as the combination of Magesacher, Barnette, and AAPA would achieve the same

predictable filtering result when combined with the teachings of Hyatt.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MICHAEL YAARY whose telephone number is

(571)270-1249. The examiner can normally be reached on Monday-Friday, 8:00 a.m -

5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. Y./
Examiner, Art Unit 2193

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193